Amendments to the Specification:

Please replace the previously replaced paragraph beginning on page 5, line 9 of the specification with the paragraph below. The paragraph is amended to correct errors in previously amending this paragraph and for clarity. Added text is underlined, deleted text has been struck through.

The external voltage available at terminal 25 is the same voltage available at terminal 11 and is also available to the NMOS transistor 47 along line 49. The internal reference voltage along line 35 is transferred to line 45 connected to the gate of transistor 47 and establishes conduction for the transistor 47 which preferably has a conduction threshold of approximately zero volts. ~~the~~ The output of transistor 47 is taken along line 51 and is another internal reference voltage feeding the high current ~~and noisy low voltage circuits~~ circuit 53. Transistor 47 feeds ~~a~~ the high current load 53 directly and can be scaled to handle sufficient current for the load. Alternatively, parallel transistors, constructed identically to transistor 47 can feed similar loads at other locations on an integrated circuit chip.

Please replace the paragraph beginning on page 7, line 23 of the specification with the paragraph below.

This paragraph is amended to correct errors identifying the external V_{cc} voltage on terminal 25. This paragraph is also amended to correct reference to the voltage supply for the low current load provided on line 35 of Fig. 1. Added text is underlined, deleted text has been struck through.

With reference to Fig. 3, one of the clock circuits with an associated capacitor, such as clock circuit 62 and adjoining capacitor 61, shown in Fig. 2, are illustrated using two regulated output voltages, shown in the circuit of Fig. 1. A first voltage is the ~~internal~~ external V_{cc} voltage shown to pass through transistor 47 to the high current load 53 in Fig. 1. In Fig. 3, transistor 47 has been redrawn from Figs. 1 and 2 and receives the ~~internal~~ external V_{cc} voltage from terminal 25, with the transistor output on line 51 going to inverter 71. The inverter is formed by the p-channel transistor 73 and n-channel transistor 75 driven by a pulse train from oscillator 77. This oscillator has a voltage supply associated with a low current load, such as the voltage ~~terminal 29~~ on line 35 in Fig. 1. The output of oscillator 77 provides a low voltage first pulse train drive to the gates of the two transistors forming the inverter 71.